OMKAR BHILARE

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EDUCATION

Veermata Jijabai Technological Institute *Mumbai, India.*
B.Tech in Electronics Engineering **[GPA: 9.13/10] [Rank: 6/74]** *July 2019 - May 2022*
**(Direct 2nd year lateral entry in 4 year Bachelor Program)*

- **Relevant Coursework:** Principle of VLSI [**10/10**], Microcomputer System Design [**10/10**], Electronics Circuit Analysis and Design [**10/10**], Digital Combinational Circuits [**10/10**], Digital Sequential Circuits [**10/10**], Microprocessor and Microcontroller[**10/10**], Microprocessor Systems [**9/10**], Embedded Systems [**10/10**]

Veermata Jijabai Technological Institute *Mumbai, India.*
Diploma in Electronics Engineering **[Percentage: 97.15%] [Rank: 1/67]** *August 2016 - June 2019*

AWARDS AND RECOGNITION

- **Adaptive Computing Challenge 2021 by AMD-Xilinx** (Third Place with a prize worth $3000) - an award winner from 165 qualified entries from developers spanning 35 countries
- Received **VCK5000—a Versal architecture-based FPGA** board as a hardware grant(worth $2700) - only 20 such boards were distributed globally among 547 applications
- ***Summer@EPFL*** scholar - Three-month summer fellowship to conduct cutting-edge research at EPFL
- Selected participant in the prestigious ***Google Summer of Code*** program—a Google-run program that focuses on bringing new contributors into open-source development

PUBLICATIONS

Conference Papers

- *DEEPFAKE CLI: Accelerated Deepfake Detection using FPGAs.* **Accepted (August 2022)**
  Omkar Bhilare, Rahul Singh, Vedant Paranjape, Sravan Chittupalli, Shraddha Suratkar, and Faruk Kazi
  Parallel and Distributed Computing, Applications and Technologies (PDCAT'22) [Preprint]

RESEARCH EXPERIENCE

Processor Architecture Laboratory (LAP), EPFL **Prof. Paolo Ienne, Mr. Andrea Guerrieri**
Summer@EPFL *June 2022 - August 2022*

- Designed a framework for Dynamatic (a dynamic HLS compiler) to access external memory using AXI interconnect [BLOG]
- Developed a custom-built AXI master with burst support and successfully tested it with load-store queues (LSQs) of Dynamatic
- Added Burst support in a highly dynamic environment of Dynamaitc using special-built BOM (Burst & Outstanding Manager) modules
- **Dynamatic's memory handling capabilities were substantially expanded by the unit, at a mere 2% LUT and 4% FF count increase**

Centre of Excellence in Complex and Non-Linear Dynamical Systems, VJTI **Prof. Faruk Kazi**
Bachelor's thesis: Accelerated Deepfake detection on VCK5000 Versal FPGA [BLOG] *June 2021 - May 2022*
Research Associate

- Trained, quantized, and compiled various AI models for Xilinx Zynq and Versal FPGA platforms
- Studied the Versal AI architecture. The Deepfake Detection AI model was quantized to INT8 and compiled for Xilinx's CNN accelerator running on VCK5000 Versal FPGA fabric, which is coupled to AI engines for enhanced performance.
- Benchmarked and achieved a **120% improvement in model inference speed** on the VCK5000 over the state-of-the-art Nvidia Tesla T4 GPU inference speed
- Impact of employing different quantization levels of a deep learning model on inference speed and optimization of Deepfake detection model for VCK5000 FPGA led to a conference paper at **The 23rd International Conference on Parallel and Distributed Computing, Applications, and Technologies** (PDCAT'22)

Shakti Lab, RISE Group, IIT Madras **Prof. V. Kamakoti, Mrs. Lavanya J**
Research Verification Intern [REPORT] *March 2021 - July 2021*

- Worked under the guidance of Prof. V. Kamakoti, who is the director of IITM and head of the SHAKTI, RISE group. They made **SHAKTI, which is India's first indigenous processor**. I designed and developed a **framework to verify the SHAKTI RISC-V processors on FPGAs**
- Developed an automation flow called *AAPG on FPGA* which automatically generates single and multiple tests produced by Automated Assembly Program Generator (AAPG), which are suitable to run on FPGA directly
- Successfully verified the framework by running a softcore VAJRA SoC on an Arty A7 FPGA. Obtained signature dumped from FPGA using OpenOCD and RISC-V GDB and compared it with the golden signature from *S*pike, a RISC-V ISA Simulator
- The proposed work **accelerated verification speed while maintaining visibility and control** in FPGA flow

WORK EXPERIENCE

AMD **Bangalore, India**
Silicon Design Engineer I *September 2022 - Present*

- Responsible for SoC Level Verification Suite of Debug Unit related IPs in various AMD Processors
- Worked on verifying the low power mode of USB with SoC level verification test. That involved putting the USB into low power mode and afterward reading the block of the ID of the USB IP over IO pads to make sure it is working

AMD **Remote**
Verification Co-op Intern *Dec 2021 - June 2022*

- Verified Debug Unit test suite at SoC Level using various constrained random test cases
- Designed and verified CPU core access test case, which was configurable enough to select one core inside AMD CPU according to the test input and check its accessibility
- Developed verification test case for CPU cross-trigger network between multiple IPs

Google Summer of Code 2021, BeagleBoard Organization **Remote**
Open-Source Developer [REPORT] *June 2021 - Aug 2021*

- Built and tested a **gateware for BeagleWire** (Lattice iCE40 FPGA) cape for Beaglebone Black (a single board computer)
- **Interfaced Arm Chip with Lattice FPGA** using General Purpose Memory Controller (GPMC) and Wishbone protocols
- Designed and verified GPMC to Wishbone converter IP. It supported single reads and writes and also included two flop synchronizer to ensure synchronization between two different clock domains
- Developed and tested Wishbone slave and Intercon designs for BeagleWire
- Interfaced BeagleWire with SDRAM using *litedram* core, which included *serv*—a bit-serial RISC-V CPU for initialization of SDRAM IP
- Designed and tested a VGA Driver for BeagleWire using VGA PMOD in hardware. Developed a gateware for the PONG game and used the VGA driver to run it on BeagleWire and a display

PROJECTS

RISC-V core github.com/riscv-core
Icarus Verilog, GTKWAVE, Yosys, Openlane, Magic, TD IDE Jan 2021 - March 2021

- Designed and verified a RISC-V core in Verilog
- For analog VLSI and tapeout process understanding, converted the basic design into silicon (GDSII) format using *Openlane* and *sky130* PDK
- Designed FPGA drivers such as VGA and others for SoC integration
- Validated the VGA driver on Tang primer FPGA with simple DAC made from binary-weighted resistors

8 Bit Computer using 74LS series ICs github.com/8-bit-computer
Logisim, Multisim May 2020 - Nov 2020

- Designed an entire 8 Bit Computer circuit using 74LS series ICs and simulated it in Logisim
- Two cascaded 74LS181 are used for the Arithmetic Logical Unit (ALU) in an 8-bit computer capable of performing 8-bit arithmetic and logical operations. It also has basic general-purpose registers and a program counter made from flipflops

SKILLS

FPGAs:	**AMD-Xilinx** (Arty, VCK5000, ZC702, Kv260), **Intel-Altera** (Cyclone II), **Lattice** (ICE40UP5K & iCE40HX4k), **Anlogic** (EG4S20)
Languages:	Verilog, VHDL, C, Python, Assembly Language(x86, RISC-V)
EDA Tools:	Quartus Prime, Xilinx Vivado, IceStorm
Software & Frameworks:	CoCotb, Icarus Verilog, GTKWave, Proteus, Multisim, Logisim, Git, Linux

TEACHING EXPERIENCE

- Lecturer at WallE - Annual workshop at robotics club called SRA, VJTI to introduce juniors to microarchitecture and FPGA prototyping
- Held a lecture in the 'Robotics' course of an undergraduate mechanical engineering degree program at VJTI to expose students to the line following using ESP32 and how microcontrollers can be used in various applications

CO-CURRICULAR ACTIVITIES

- Served as a Joint General Secretary of SRA (Aug 2019 - June 2022) and mentored many students in computer-architecture-related domains
- Got accepted into NSM-Computer Architecture Winter School 2021—a two-week winter school to provide an introduction to basic and advanced topics in Computer Architecture which included speakers from IIT Bombay, IIT Madras, IIT Delhi, AMD, and Microsoft [Certificate]
- Tested and published a technical blog (over 3000 views) on RA2L1 EVK (Ultra-Low Power 48MHz Arm Cortex-M23) sample board from the element14 RoadTest program